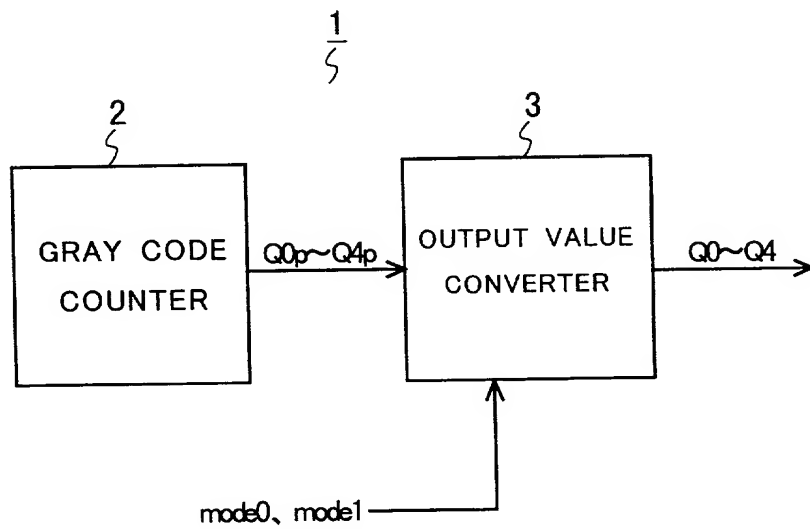


Fig. 1



PRIOR ART

Fig. 2

DECIMAL COUNT	BINARY CODE	GRAY CODE
0	00000	00000
1	00001	00001
2	00010	00011
3	00011	00010
4	00100	00110
5	00101	00111
6	00110	00101
7	00111	00100
8	01000	01100
9	01001	01101
10	01010	01111
11	01011	01110
12	01100	01010
13	01101	01011
14	01110	01001
15	01111	01000
16	10000	11000
17	10001	11001
18	10010	11011
19	10011	11010
20	10100	11110
21	10101	11111
22	10110	11101
23	10111	11100
24	11000	10100
25	11001	10101
26	11010	10111
27	11011	10110
28	11100	10010
29	11101	10011
30	11110	10001
31	11111	10000

20050101 013000

Fig. 3

DECIMAL COUNT	GRAY CODE	GRAY CODE HIGHEST 4 BITS	GRAY CODE LOWEST BIT
0	00000	0000	0
2	00011	0001	1
4	00110	0011	0
6	00101	0010	1
8	01100	0110	0
10	01111	0111	1
12	01010	0101	0
14	01001	0100	1
16	11000	1100	0
18	11011	1101	1
20	11110	1111	0
22	11101	1110	1
24	10100	1010	0
26	10111	1011	1
28	10010	1001	0
30	10001	1000	1

Fig. 4

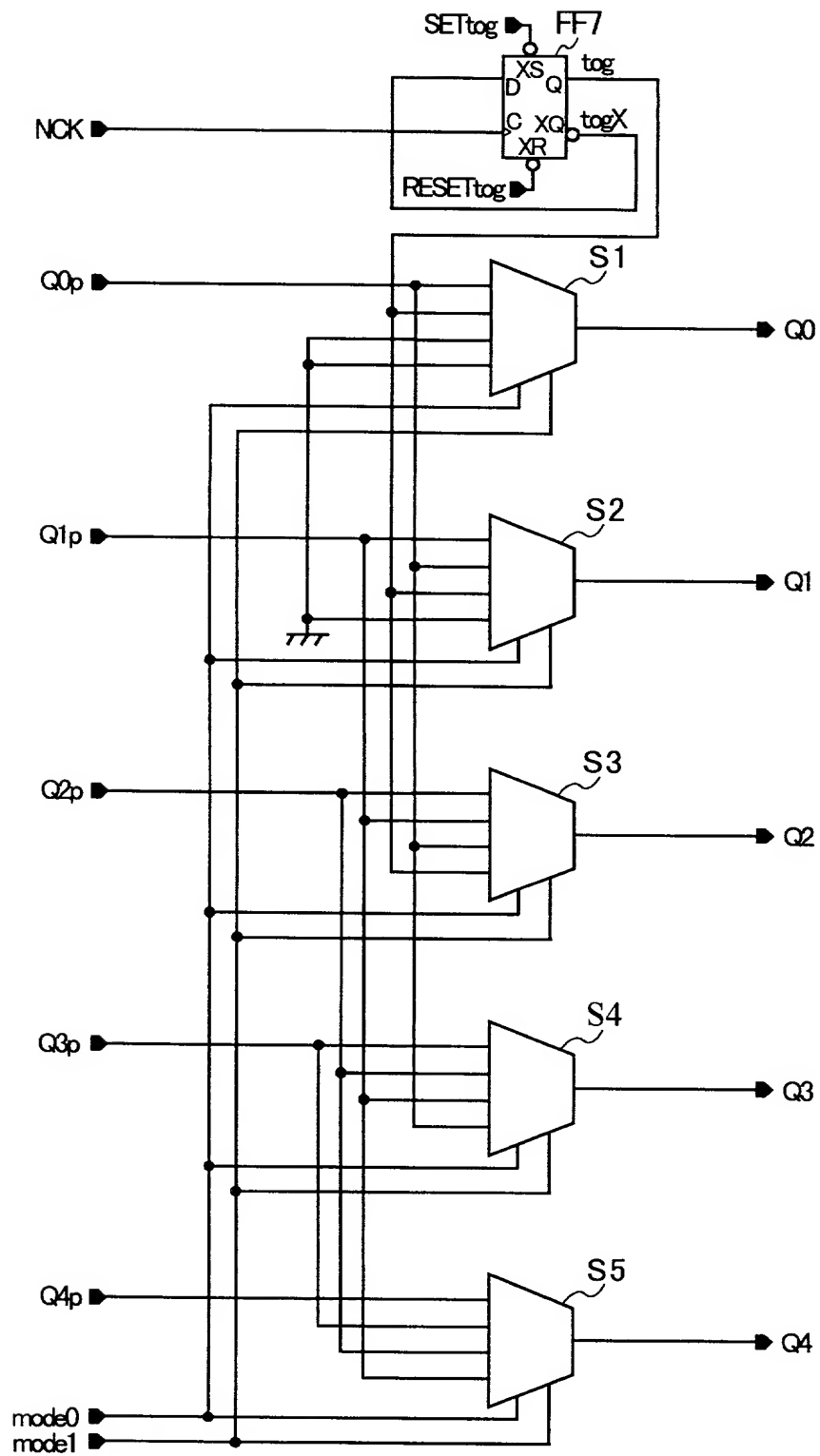
DECIMAL COUNT	GRAY CODE	GRAY CODE HIGHEST 3 BITS	GRAY CODE FIRST BITS	GRAY CODE LOWEST BIT
0	00000	000	0	0
4	00110	001	1	0
8	01100	011	0	0
12	01010	010	1	0
16	11000	110	0	0
20	11110	111	1	0
24	10100	101	0	0
28	10010	100	1	0

Fig. 5

DECIMAL COUNT	GRAY CODE	GRAY CODE HIGHEST 2 BITS	GRAY CODE SECOND BITS	GRAY CODE FIRST BITS	GRAY CODE LOWEST BIT
0	00000	00	0	0	0
8	01100	01	1	0	0
16	11000	11	0	0	0
24	10100	10	1	0	0

Fig. 6

3



F i g . 7

CONTROL SIGNALS		OUTPUT BIT DATA					COUNT OPERATION
mode1	mode0	Q4	Q3	Q2	Q1	Q0	
0	0	Q4p	Q3p	Q2p	Q1p	Q0p	CONSECUTIVE
0	1	Q3p	Q2p	Q1p	Q0p	tog	1 COUNT SKIPPED
1	0	Q2p	Q1p	Q0p	tog	0	3 COUNTS SKIPPED
1	1	Q1p	Q0p	tog	0	0	7 COUNTS SKIPPED

200ET0" 98E8500T

Fig. 8

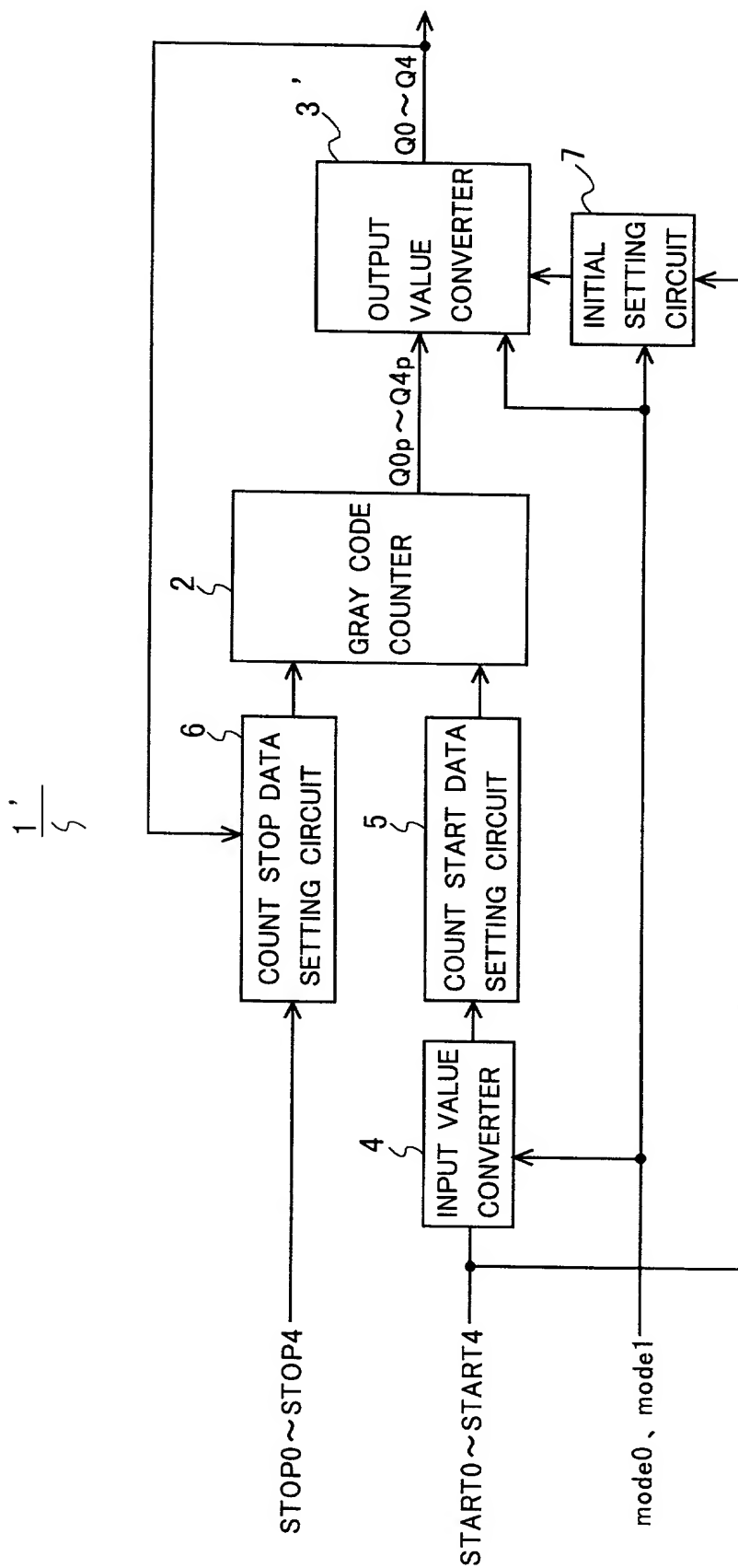


Fig. 9

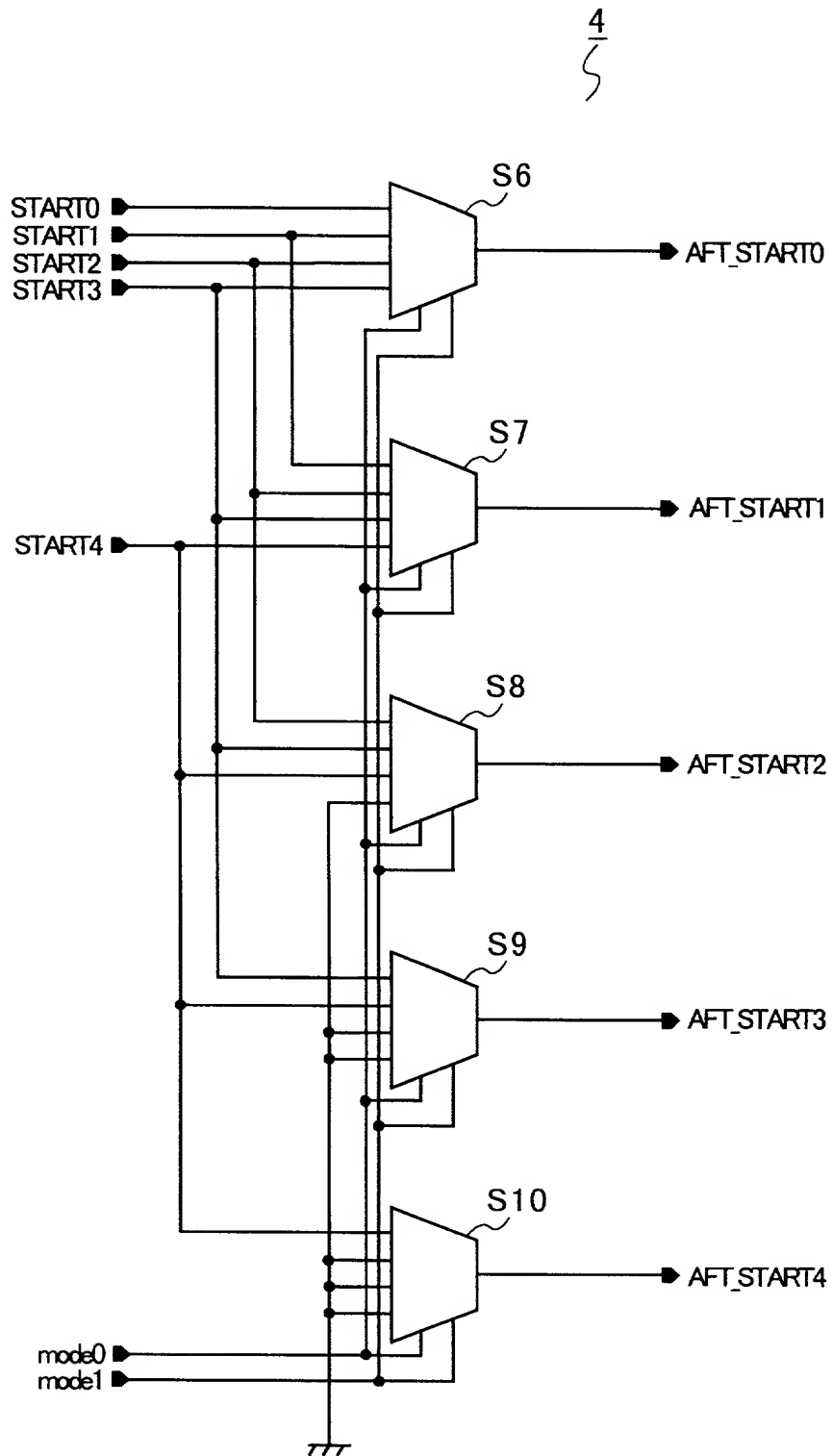


Fig. 10

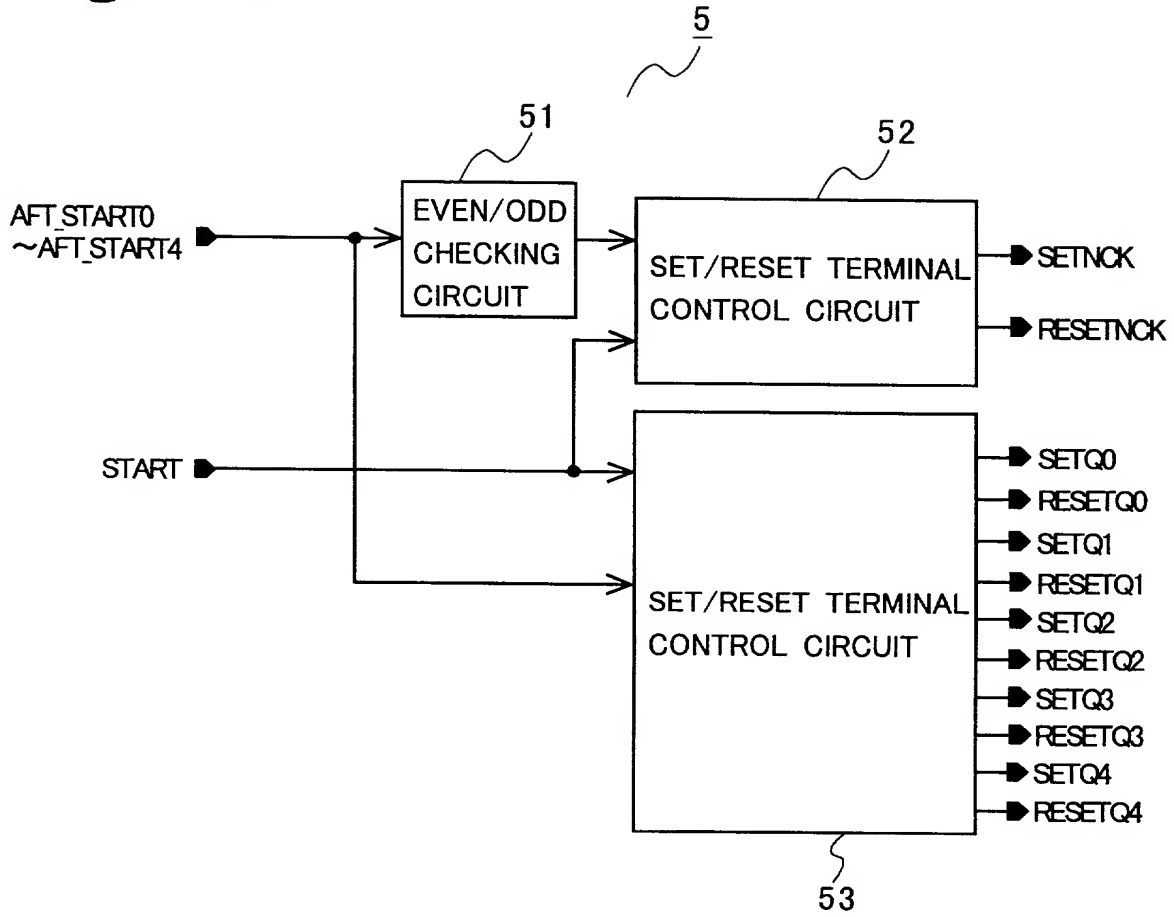


Fig. 11

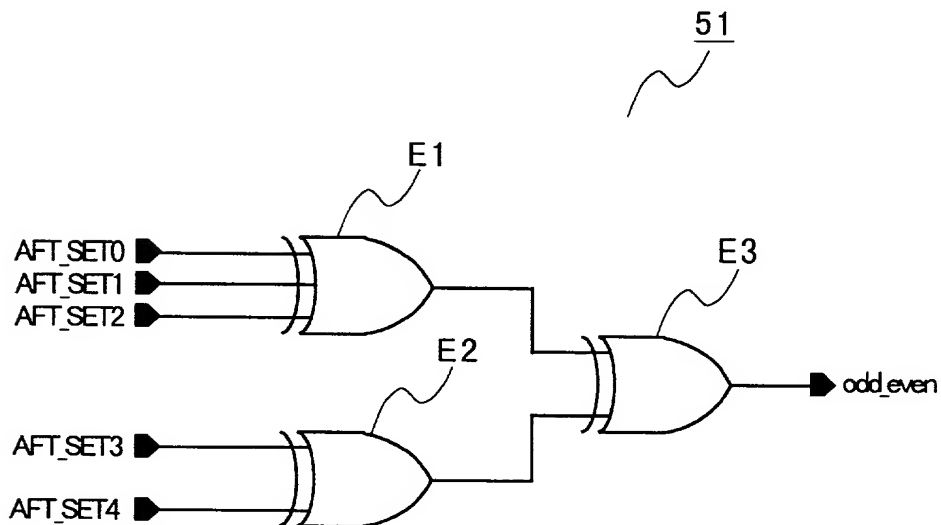


Fig. 12

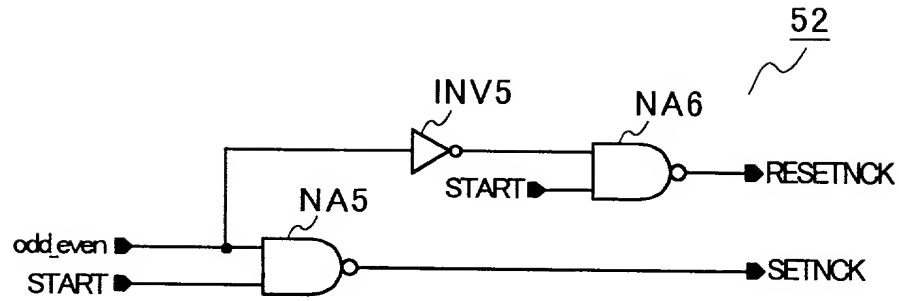
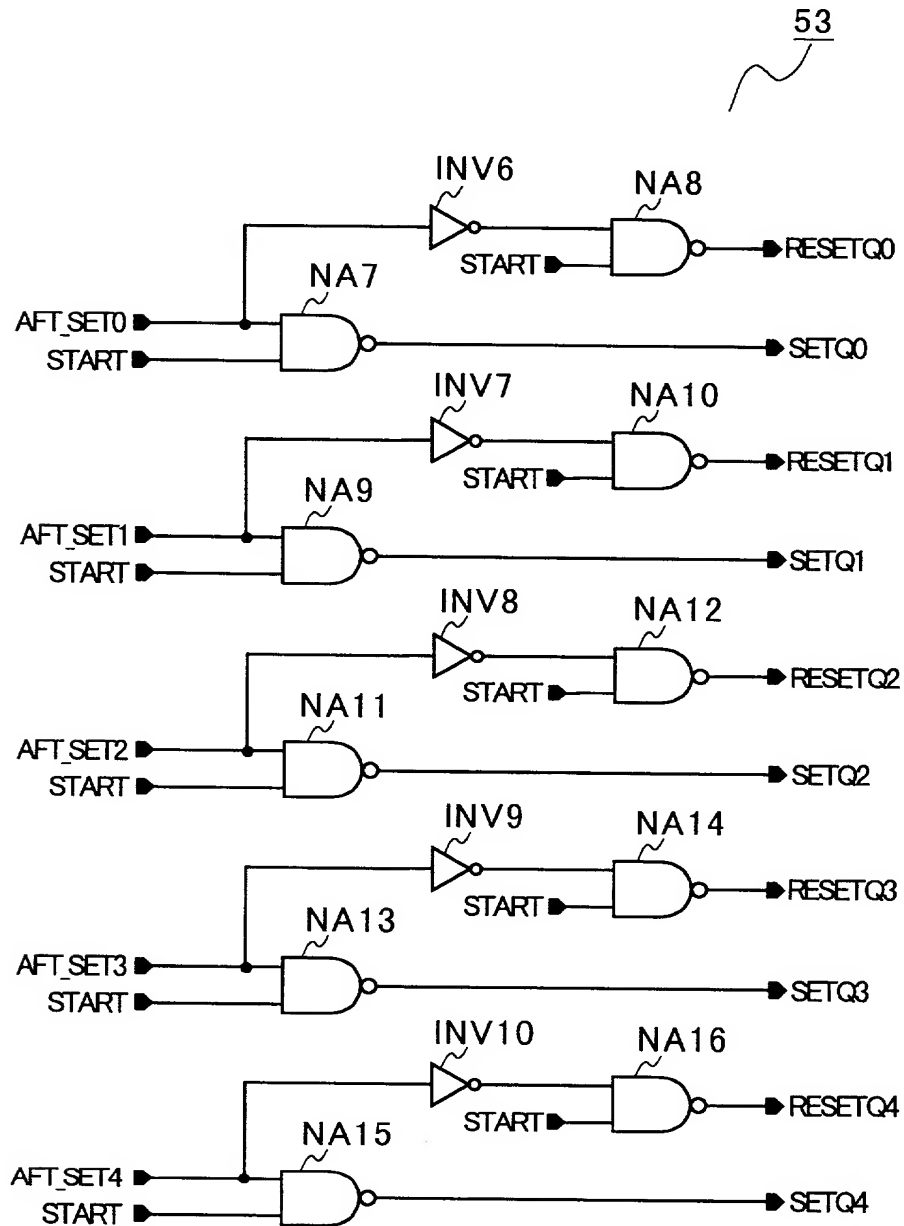


Fig. 13



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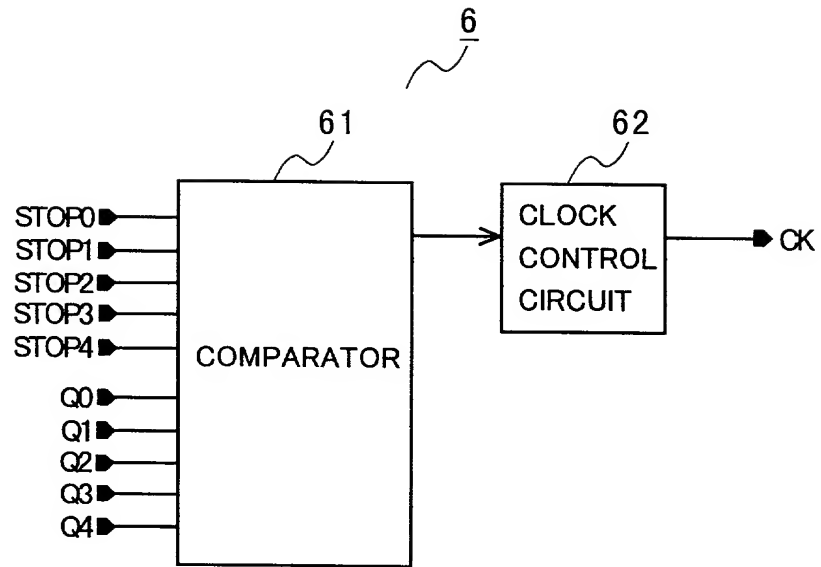


Fig. 15

3'

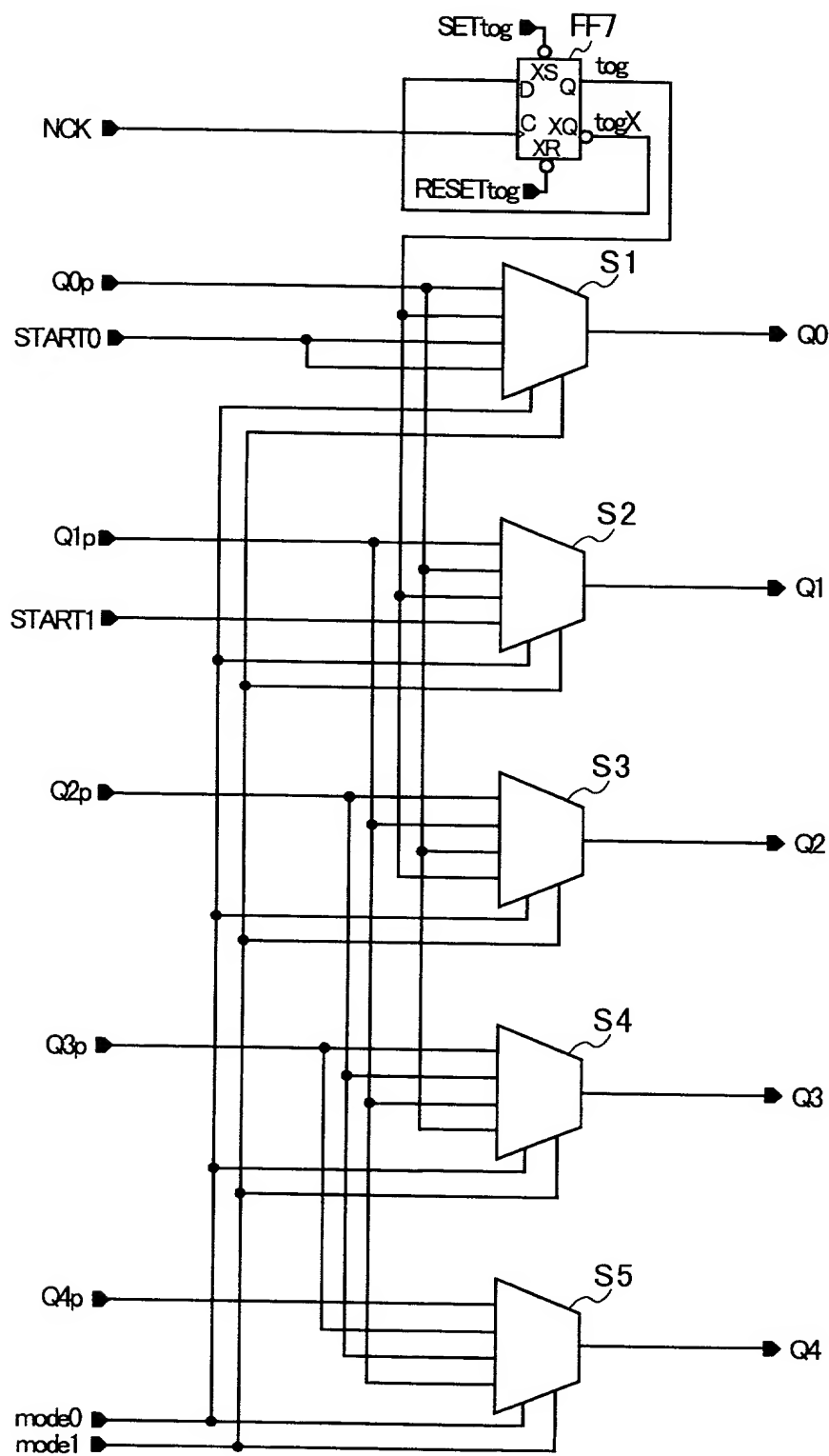


Fig. 16

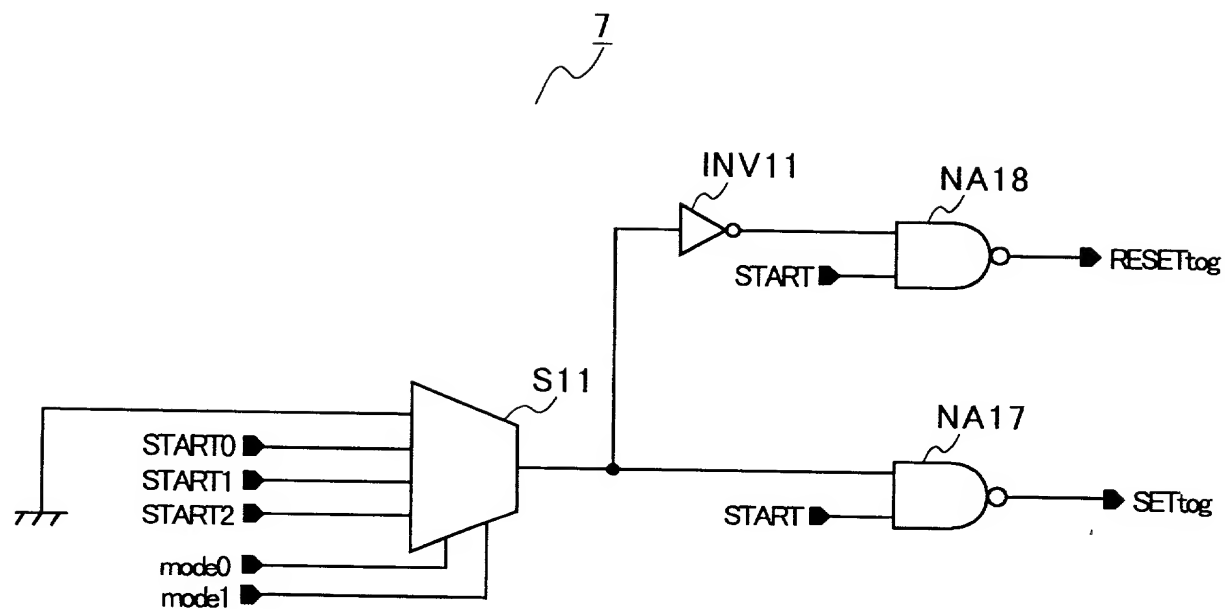


Fig. 17A

DECIMAL COUNT	GRAY CODE HIGHEST 4 BITS	GRAY CODE LOWEST BIT
0	0000	0
2	0001	1
4	0010	0
6	0011	1
8	0100	0
10	0101	1
12	0110	0
14	0111	1
16	1000	0
18	1001	1
20	1010	0
22	1011	1
24	1100	0
26	1101	1
28	1110	0
30	1111	1

Fig. 17B

DECIMAL COUNT	GRAY CODE HIGHEST 4 BITS	GRAY CODE LOWEST BIT
1	0000	1
3	0001	0
5	0010	1
7	0011	0
9	0100	1
11	0101	0
13	0110	1
15	0111	0
17	1000	1
19	1001	0
21	1010	1
23	1011	0
25	1100	1
27	1101	0
29	1110	1
31	1111	0

Fig. 18A

DECIMAL COUNT	GRAY CODE HIGHEST 3 BITS	GRAY CODE FIRST BIT	GRAY CODE LOWEST BIT
0	0000	0	0
4	0010	1	0
8	0100	0	0
12	0110	1	0
16	1000	0	0
20	1010	1	0
24	1100	0	0
28	1110	1	0

Fig. 18B

DECIMAL COUNT	GRAY CODE HIGHEST 3 BITS	GRAY CODE FIRST BIT	GRAY CODE LOWEST BIT
1	0001	0	1
5	0011	1	1
9	0101	0	1
13	0111	1	1
17	1001	0	1
21	1011	1	1
25	1101	0	1
29	1111	1	1

Fig. 18C

DECIMAL COUNT	GRAY CODE HIGHEST 3 BITS	GRAY CODE FIRST BIT	GRAY CODE LOWEST BIT
2	0001	1	1
6	0010	0	1
10	0100	1	1
14	0110	0	1
18	1000	1	1
22	1010	0	1
26	1100	1	1
30	1110	0	1

Fig. 18D

DECIMAL COUNT	GRAY CODE HIGHEST 3 BITS	GRAY CODE FIRST BIT	GRAY CODE LOWEST BIT
3	0001	1	0
7	0010	0	0
11	0100	1	0
15	0110	0	0
19	1000	1	0
23	1010	0	0
27	1100	1	0
31	1110	0	0

Fig. 19

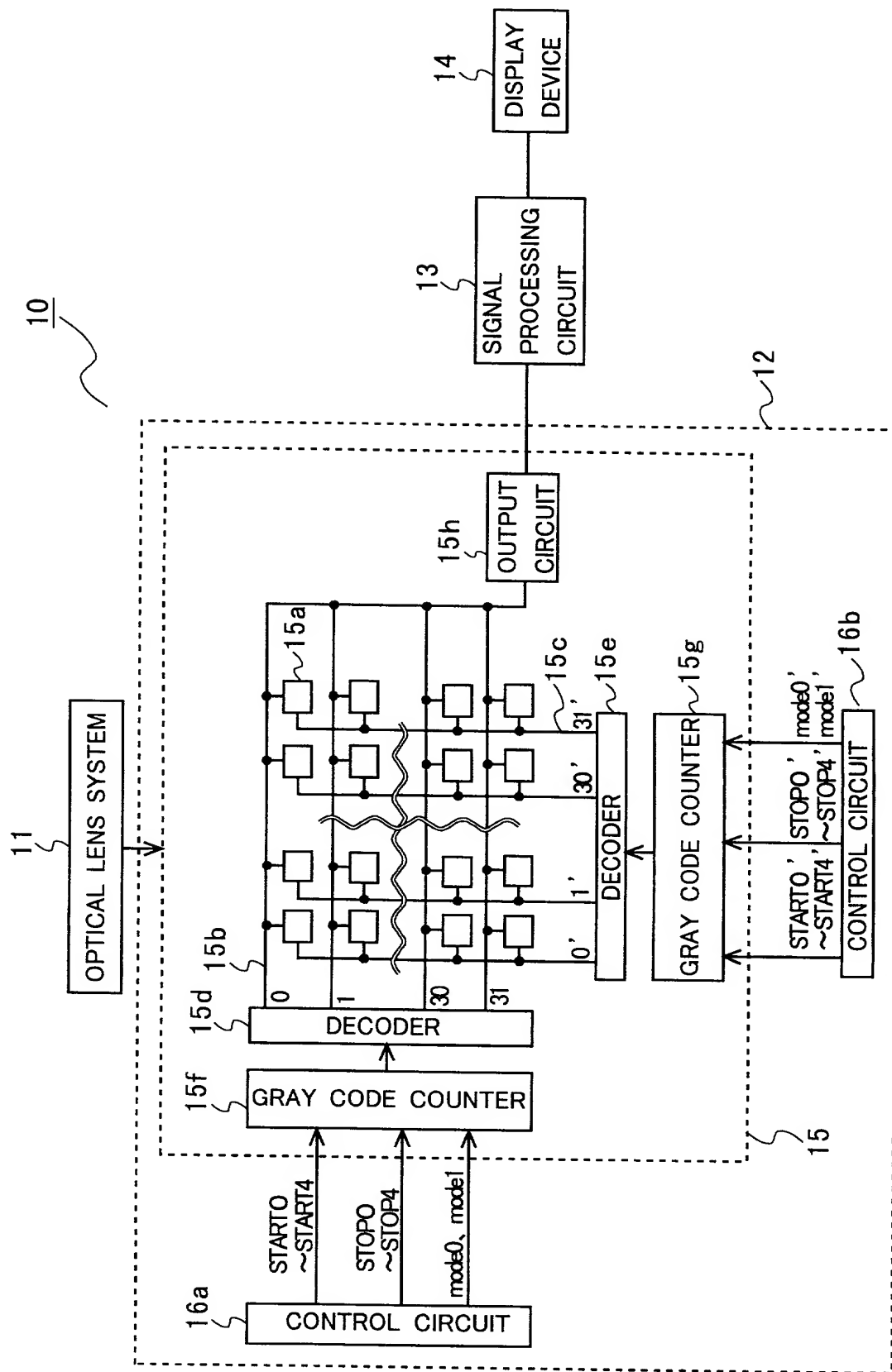
CONTROL SIGNALS		OUTPUT BIT DATA					COUNT OPERATION
mode1	mode0	Q4	Q3	Q2	Q1	Q0	
0	0	Q4p	Q3p	Q2p	Q1p	Q0p	CONSECUTIVE
0	1	Q3p	Q2p	Q1p	Q0p	tog	1 COUNT SKIPPED
1	0	Q2p	Q1p	Q0p	tog	START0	3 COUNTS SKIPPED
1	1	Q1p	Q0p	tog	START1	START0	7 COUNTS SKIPPED

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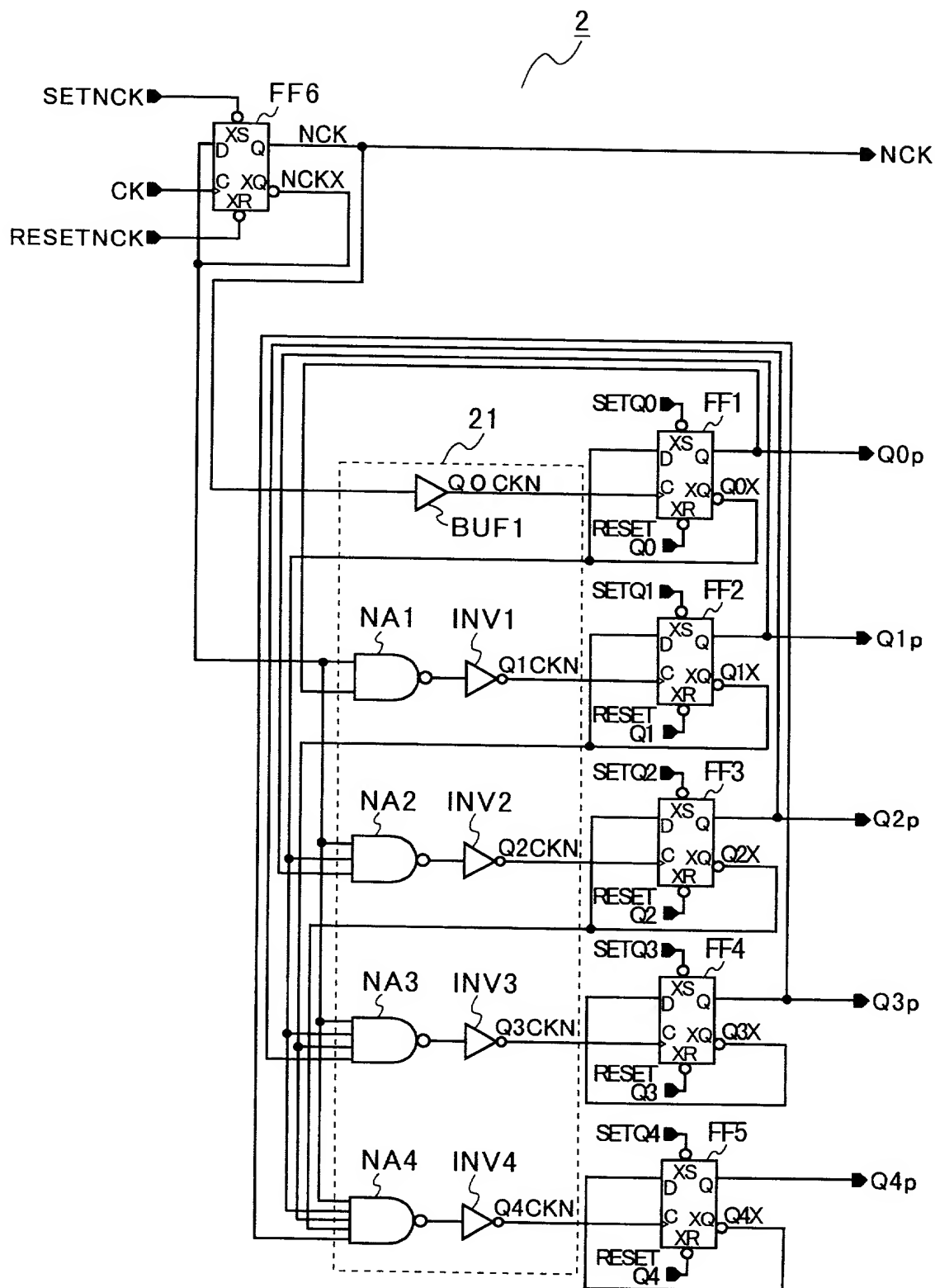
Fig. 20

CONTROL SIGNALS		INPUT VALUE CONVERTER OUTPUT BIT DATA					COUNT OPERATION
mode1	mode0	AFT_START4	AFT_START3	AFT_START2	AFT_START1	AFT_START0	
0	0	START4	START3	START2	START1	START0	CONSECUTIVE
0	1	0	START4	START3	START2	START1	1 COUNT SKIPPED
1	0	0	0	START4	START3	START2	3 COUNTS SKIPPED
1	1	0	0	0	START4	START3	7 COUNTS SKIPPED

Fig. 21



PRIOR ART Fig. 22



PRIOR ART
Fig. 23

